

PATENT COOPERATION TREATY

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

From the INTERNATIONAL BUREAU

To:

Commissioner
US Department of Commerce
United States Patent and Trademark
Office, PCT
2011 South Clark Place Room
CP2/5C24
Arlington, VA 22202
ETATS-UNIS D'AMERIQUE
in its capacity as elected Office

Date of mailing (day/month/year) 06 February 2001 (06.02.01)	
International application No. PCT/EP00/05148	Applicant's or agent's file reference CE50036P/PCT/LML
International filing date (day/month/year) 01 June 2000 (01.06.00)	Priority date (day/month/year) 01 June 1999 (01.06.99)
Applicant HIETALA, Alex et al	

1. The designated Office is hereby notified of its election made:

☒ in the demand filed with the International Preliminary Examining Authority on:
20 December 2000 (20.12.00)

☐ in a notice effecting later election filed with the International Bureau on:

2. The election ☒ was
☐ was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No.: (41-22) 740.14.35	Authorized officer R. E. Stoffel Telephone No.: (41-22) 338.83.38
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PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference CE50036P/PCT/LML	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/EP 00/ 05148	International filing date (day/month/year) 01/06/2000	(Earliest) Priority Date (day/month/year) 01/06/1999
Applicant MOTOROLA INC.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

- a. With regard to the language, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

- b. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international search was carried out on the basis of the sequence listing :

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. ☐ Certain claims were found unsearchable (See Box I).

3. ☐ Unity of invention is lacking (see Box II).

4. With regard to the title,

☐ the text is approved as submitted by the applicant.

☒ the text has been established by this Authority to read as follows:

MULTIPLIER FOR MULTIPLYING COMPLEX SIGNALS

5. With regard to the abstract,

☐ the text is approved as submitted by the applicant.

☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the drawings to be published with the abstract is Figure No.

☒ as suggested by the applicant.

☐ because the applicant failed to suggest a figure.

☐ because this figure better characterizes the invention.

1
☐ Non of the figures.

INTERNATIONAL SEARCH REPORT

ational application No.

PCT/EP 00/05148

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

PLEASE CHANGE:

A COMPLEX MULTIPLIER (51) FOR USE IN A RADIO RECEIVER (20,30,50,60)....UNTIL
LINE 5:SPACING. CONTINUE: THE RECEIVER INCLUDES A LOCAL OSCILLATOR....UNTIL
LINE 10, ADD AT THE END "COMPRISES", FINISH WITH THE ORIGINAL.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 00/05148

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H03D3/00		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) IPC 7 H03D		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the International search (name of data base and, where practical, search terms used) PAJ		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	* WO 97 08842 A (PACIFIC COMM SCIENCES INC) 6 March 1997 (1997-03-06) claims 12-14; figure 4A ---	1-4,7
X	US 5 878 089 A (DAPPER MARK J ET AL) 2 March 1999 (1999-03-02) column 4, line 11 -column 5, line 20; figure 2 ---	1-3,7
A	US 4 688 096 A (CAMPBELL III EDWARD R ET AL) 18 August 1987 (1987-08-18) figures 1,3 ---	1,7
A	* WO 94 29948 A (RCA THOMSON LICENSING CORP ;ASCHWANDEN FELIX (CH)) 22 December 1994 (1994-12-22) abstract; figure 5 --- -/--	4
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C. <input checked="" type="checkbox"/> Patent family members are listed in annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
Date of the actual completion of the international search 8 September 2000		Date of mailing of the international search report 20/09/2000
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Peeters, M

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 00/05148

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	* WO 98 08300 A (ADVANCED MICRO DEVICES INC) 26 February 1998 (1998-02-26) page 10, line 39 -page 11, line 13 ---	9
A	US 5 777 521 A (BUSHMAN MICHAEL L ET AL) 7 July 1998 (1998-07-07) figure 4 ---	10,11
A	US 5 625 359 A (SOBOL JAMES M ET AL) 29 April 1997 (1997-04-29) abstract -----	12

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP 00/05148

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9708842 A	06-03-1997	US 5828955 A	27-10-1998
US 5878089 A	02-03-1999	NONE	
US 4688096 A	18-08-1987	DE 3718103 A	03-12-1987
		FR 2599574 A	04-12-1987
		GB 2191367 A,B	09-12-1987
		HK 41395 A	31-03-1995
		JP 2627270 B	02-07-1997
		JP 62287781 A	14-12-1987
		KR 9504103 B	25-04-1995
		SG 28693 G	21-05-1993
WO 9429948 A	22-12-1994	CN 1125016 A	19-06-1996
		DE 69420727 D	21-10-1999
		DE 69420727 T	05-01-2000
		EP 0701745 A	20-03-1996
		US 5999802 A	07-12-1999
		SG 24123 A	10-02-1996
		TR 27845 A	31-08-1995
WO 9808300 A	26-02-1998	US 5802463 A	01-09-1998
		DE 69701635 D	11-05-2000
		EP 0920729 A	09-06-1999
US 5777521 A	07-07-1998	WO 9908386 A	18-02-1999
US 5625359 A	29-04-1997	US 5619202 A	08-04-1997
		DE 69510083 D	08-07-1999
		DE 69510083 T	05-01-2000
		EP 0793876 A	10-09-1997
		WO 9616482 A	30-05-1996
		US 5625358 A	29-04-1997
		US 5528240 A	18-06-1996
		US 5574454 A	12-11-1996
		US 5552785 A	03-09-1996

PATENT COOPERATION TREATY

PCT

REC'D 20 SEP 2001

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

13

Applicant's or agent's file reference CE50036P	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/EP00/05148	International filing date (day/month/year) 01/06/2000	Priority date (day/month/year) 01/06/1999
International Patent Classification (IPC) or national classification and IPC H03D3/00		
Applicant MOTOROLA INC. et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.



2. This REPORT consists of a total of 5 sheets, including this cover sheet.

- ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☒ Certain defects in the international application
- VIII ☒ Certain observations on the international application

Date of submission of the demand 20/12/2000	Date of completion of this report 18.09.2001
Name and mailing address of the international preliminary examining authority:  European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Fritzsche, H-V Telephone No. +49 89 2399 2394 

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP00/05148

I. Basis of the report

1. With regard to the **elements** of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17)*):

Description, pages:

1-13 as originally filed

Claims, No.:

1-13 as originally filed

Drawings, sheets:

1/3-3/3 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP00/05148

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims
	No:	Claims 1,2,3,4,7
Inventive step (IS)	Yes:	Claims 6
	No:	Claims 5,8-13
Industrial applicability (IA)	Yes:	Claims 1-13
	No:	Claims

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re It m V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following document/s/:
D1: WO 97 08842 A (PACIFIC COMM SCIENCES INC) 6 March 1997 (1997-03-06)
D2: US-A-5 878 089 (DAPPER MARK J ET AL) 2 March 1999 (1999-03-02)
2. The document D1 is regarded as being the closest prior art to the subject-matter of claim 1, and discloses (the references in parentheses applying to this document, see especially Fig. 2 and 4C):
A complex multiplier for multiplying together a first input complex signal, having an In-phase, I, component and a Quadrature-phase, Q, component, and a second input complex signal and generating an output complex signal which is the product of the first and second input signals, the complex multiplier including a gain adjustment multiplier (Fig.4C, means 48,50,46) for adjusting the gain of one of the first signal's I and Q components relative to the other and a phase adjustment adder (Fig. 4C, means 40', 56a,52b, 52c) for adjusting the phase of one of the first signal's I and Q components relative to the other. Consequently, the subject-matter of **claim 1** is not new and does not therefore meet the requirements of Article 33(2) of the PCT.
3. The features of **claim 2** are known from document D1, Fig.2 (DSP).
The features of **claim 3** are known from document D1, Fig..4C, DDS 56a, $\sin((wt)+\phi)$, $\cos((wt)+\phi)$.
The features of **claim 4** are known from document D1, Fig..4C, DDS 56a, $\sin((wt)+\phi)$, $\cos((wt)+\phi)$.
The features of **claim 7** are known from document D1, page 1, Fig.2.
Consequently, the subject-matter of **claims 2,3,4 and 7** is not new and does not therefore meet the requirements of Article 33(2) of the PCT.

In the description, page 13, it is stated that the higher order realisation could be done by a non specific digital processor. The man skilled in the art will do so if higher quality is necessary. Consequently the features of **claim 5** are only a

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT - SEPARATE SHEET**

International application No. PCT/EP00/05148

simple measure. Thus, the subject-matter of **claim 5** does not involve an inventive step and does not satisfy the criterion set forth in Article 33(3) PCT.

4. The features of **claim 6** appear to support an inventive step.
5. The features of **claim 8** are vague and only represent a result. They cannot support an inventive step.
The other dependent claims contain only minor features known from document D1 or well known to the man skilled in the art.
The subject-matter of **claims 8-13** is accordingly lacking inventive step contrary to Article 33(3), PCT.

Re Item VII

Certain defects in the international application

The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the document/s D1, D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

Claim 4 is not clear. In claim 4 the definition of the phase adjustment adder is not clear. Where is the adder in the Figures? The applicant is asked to give the corresponding reference sign.

PCT REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No. PCT/EP 00 / 05148
International Filing Date 01 JUN 2000 (01.06.00)
EUROPEAN PATENT OFFICE PCT INTERNATIONAL APPLICATION
Applicant's or agent's file reference (if desired) (12 characters maximum) CE50036P/PCT/LML

Box No. I	TITLE OF INVENTION COMPLEX MULTIPLIER	
Box No. II	APPLICANT	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) Motorola Inc. 1303 E. Algonquin Road, Schaumburg 60196 Illinois, United States Of America		<input type="checkbox"/> This person is also inventor. Telephone No. Facsimile No. Teleprinter No.
State (i.e. country) of nationality: US ^{AA}		State (i.e. country) of residence: US ^{AA}
This person is applicant <input type="checkbox"/> all designated States <input checked="" type="checkbox"/> all designated States except the United States of America <input type="checkbox"/> the United States of America only <input type="checkbox"/> the States indicated in the Supplemental Box		
Box No. III	FURTHER APPLICANTS AND/OR (FURTHER) INVENTORS	
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) HIETALA, Alex 14017 South 9th Street, Phoenix Arizona 85048 U.S.A. ^{AA}		This person is: <input type="checkbox"/> Applicant only <input checked="" type="checkbox"/> applicant and inventor <input type="checkbox"/> inventor only (if this check-box is marked, do not fill in below.)
State (i.e. country) of nationality: US ^{AA}		State (i.e. country) of residence: US ^{AA}
This person is applicant <input type="checkbox"/> all designated States <input type="checkbox"/> all designated States except the United States of America <input checked="" type="checkbox"/> the United States of America only <input type="checkbox"/> the States indicated in the Supplemental Box		
<input checked="" type="checkbox"/> Further applicants and/or (further) inventors are indicated on a continuation sheet.		
Box No. IV	AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE	
The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:		
<input checked="" type="checkbox"/> agent <input type="checkbox"/> common representative		
Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country) LITCHFIELD, Laura Motorola European Intellectual Property Operations Midpoint, Alencon Link, Basingstoke, Hampshire RG21 7PL GB ^A		Telephone No. 01256 790384 Facsimile No. 01256 811319 Teleprinter No.
<input type="checkbox"/> Address for correspondence: Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.		

Form PCT/RO/101 (first sheet) (July 1998)

See Notes to the request form

CONFIRMATION COPY

Sheet number 2

Continuation of Box No. III FURTHER APPLICANTS AND/OR (FURTHER) INVENTORS	
If none of the following sub-boxes is used, this sheet is not to be included in the request.	
Name and address: (Family name followed by given name: for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) KHLAT, Nadim 24, Rue Pierre de Fermat 31270 CUGNAUX, France	This person is: <input type="checkbox"/> applicant only <input checked="" type="checkbox"/> applicant and inventor <input type="checkbox"/> inventor only (if this check-box is marked, do not fill in below.)
State (i.e. country) of nationality: FRANCE	State (i.e. country) of residence: FRANCE
This person is applicant <input type="checkbox"/> all designated <input type="checkbox"/> all designated States except <input checked="" type="checkbox"/> the United States <input type="checkbox"/> the States indicated for the purposes of: States the United States of America of America only in the Supplemental Box	
Name and address: (Family name followed by given name: for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) CLEMENT, Patrick Chemin de la Potteilaz, 111 1030 BUSSIGNY Switzerland	This person is: <input type="checkbox"/> applicant only <input checked="" type="checkbox"/> applicant and inventor <input type="checkbox"/> inventor only (if this check-box is marked, do not fill in below.)
State (i.e. country) of nationality: SWITZERLAND	State (i.e. country) of residence: SWITZERLAND
This person is applicant <input type="checkbox"/> all designated <input type="checkbox"/> all designated States except <input checked="" type="checkbox"/> the United States <input type="checkbox"/> the States indicated for the purposes of: States the United States of America of America only in the Supplemental Box	
Name and address: (Family name followed by given name: for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.) KURBY, Christopher 120 E Madison Street, Elmhurst, Illinois 60126 USA	This person is: <input type="checkbox"/> applicant only <input checked="" type="checkbox"/> applicant and inventor <input type="checkbox"/> inventor only (if this check-box is marked, do not fill in below.)
State (i.e. country) of nationality: USA	State (i.e. country) of residence: USA
This person is applicant <input type="checkbox"/> all designated <input type="checkbox"/> all designated States except <input checked="" type="checkbox"/> the United States <input type="checkbox"/> the States indicated for the purposes of: States the United States of America of America only in the Supplemental Box	
Name and address: (Family name followed by given name: for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)	This person is: <input type="checkbox"/> applicant only <input type="checkbox"/> applicant and inventor <input type="checkbox"/> inventor only (if this check-box is marked, do not fill in below.)
State (i.e. country) of nationality:	State (i.e. country) of residence:
This person is applicant <input type="checkbox"/> all designated <input type="checkbox"/> all designated States except <input type="checkbox"/> the United States <input type="checkbox"/> the States indicated for the purposes of: States the United States of America of America only in the Supplemental Box	
<input type="checkbox"/> Further applicants and/or (further) inventors are indicated on a continuation sheet.	

Sheet number 5

Box No. VI PRIORITY CLAIM		Further priority claims are indicated in the Supplemental Box <input type="checkbox"/>	
Priority of the following earlier application(s) is claimed:		Office where earlier application filed	
Filing Date of earlier application (day/month/year)	Number of earlier application	National application = country; regional application = regional Office	International application = receiving Office
item (1) <u>01.06.99</u> 1 June 1999	99401319.1	EP <input checked="" type="checkbox"/>	
item (2)			
item (3)			


- ☒ The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) (only if the earlier application was filed with the Office which for the purposes of the present international application is the receiving Office) identified above as item(s): (1)
- * Where the earlier application is an ARIPO application, it is mandatory to indicate in the Supplemental Box at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed (Rule 4.10(b)(ii). See Supplemental Box.

Box No. VII INTERNATIONAL SEARCHING AUTHORITY			
Choice of International Searching Authority (ISA) (if two or more International Searching Authorities are competent to carry out the international search, indicate the Authority chosen; the two-letter code may be used): <u>ISA/ EP</u>			
Request to use results of earlier search; reference to that search (if an earlier search has been carried out by or requested from the International Searching Authority):			
Date (day/month/year)	Number:	Country (or regional office):	
<u>5/11/99</u>	<u>99401319.1</u>	<u>EP</u>	

Box No. VIII CHECK LIST; LANGUAGE OF FILING	
This international application contains the following number of sheets: 1. request : 5 sheets 2. description (excluding sequence listing part) : 13 sheets 3. claims : 2 sheets 4. abstract : 1 sheet 5. drawings : 3 sheets 6. sequence listing part of description : sheets Total : <u>19</u> sheets <u>24</u>	This international application is accompanied by the item(s) marked below: 1. <input checked="" type="checkbox"/> fee calculation sheet 2. <input type="checkbox"/> separate signed power of attorney 3. <input type="checkbox"/> copy of general power of attorney 4. <input type="checkbox"/> statement explaining lack of signature 5. <input type="checkbox"/> priority document(s) identified in Box No. VI as item(s): 6. <input type="checkbox"/> translation of international application into (language): 7. <input type="checkbox"/> separate indications concerning deposited microorgs./biological mat. 8. <input type="checkbox"/> nucleotide and/or amino acid sequence listing in computer readable form 9. <input type="checkbox"/> other (specify): copy, U.S. assignment

Figure No. 1 of the drawings (if any) should accompany the abstract when it is published.

Language of filing of the international application: ENGLISH

Box No. IX SIGNATURE OF APPLICANT OR AGENT	
Next to each signature, indicate the name of the person signing and the capacity in which the person signs (if such capacity is not obvious from reading the request)	
 MITCHFIELD, Laura	

For receiving Office use only

1. Date of actual receipt of the purported international application:	<u>01 JUN 2000</u> (<u>01.06.00</u>)	2. Drawings: <input checked="" type="checkbox"/> received: <input type="checkbox"/> not received:
3. Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application:		
4. Date of timely receipt of the required corrections under PCT Article II(2):		
5. International Searching Authority specified by the applicant: <u>ISA/</u>	6. <input type="checkbox"/> Transmittal of search copy delayed until search fee is paid	

For International Bureau use only

Date of receipt of the record copy by the International Bureau:

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
7 December 2000 (07.12.2000)

PCT

(10) International Publication Number
WO 00/74230 A1

(51) International Patent Classification⁷: H03D 3/00

KURBY, Christopher [US/US]; 120 E Madison Street,
Elmhurst, IL 60126 (US).

(21) International Application Number: PCT/EP00/05148

(22) International Filing Date: 1 June 2000 (01.06.2000)

(74) Agents: LITCHFIELD, Laura et al.; Motorola European
Intellectual Property Operations, Midpoint, Alencon Link,
Basingstoke, Hampshire RG21 7PL (GB).

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
99401319.1 1 June 1999 (01.06.1999) EP

(81) Designated States (*national*): AL, AM, AT, AU, AZ, BA,
BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES,
FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP,
KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN,
MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK,
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(71) Applicant (*for all designated States except US*): MO-
TOROLA INC. [US/US]; 1303 E. Algonquin Road,
Schaumburg, IL 60196 (US).

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(72) Inventors; and

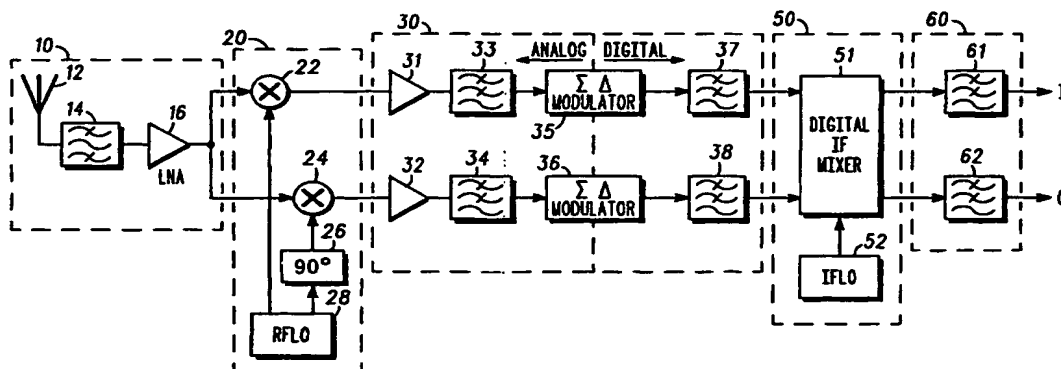
(75) Inventors/Applicants (*for US only*): HIETALA, Alex
[US/US]; 14017 South 9th Street, Phoenix, AZ 85048
(US). KHLAT, Nadim [FR/FR]; 24, rue Pierre de Fermat,
F-31270 Cugnaux (FR). CLEMENT, Patrick [CH/CH];
Chemin de la Pottelaz 111, CH-1030 Bussigny (CH).

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(54) Title: MULTIPLIER FOR MULTIPLYING COMPLEX SIGNALS



(57) Abstract: A complex multiplier (51) for use in a radio receiver (20, 30, 50, 60) for receiving a carrier signal modulated by a wanted signal, the modulated carrier signal occupying one of a plurality of channels whose central frequencies are separated from one another by a fixed frequency referred to as the channel spacing. The receiver includes a local oscillator (28) for generating first and second signals at a frequency which is not an integral multiple of half the channel spacing whereby when the received carrier signal is mixed with the first and second signals, a complex, digital Very Low Intermediate Frequency (VLIF) signal is generated in which the wanted signal is centred about a VLIF which is slightly larger than half the channel spacing. The complex multiplier comprises phase and gain adjustment means for balancing the phase and gain of the I and Q components of the VLIF signal prior to or during its down-conversion to base-band.

MULTIPLIER FOR MULTIPLYING COMPLEX SIGNALS
Field of the Invention

5 The present invention relates to a complex multiplier, and in particular to a radio receiver incorporating such a complex multiplier, for use in a portable communications device, in which the radio signal to be received is directly down converted to a complex Very Low Intermediate Frequency (VLIF) signal, having In-phase (I) and Quadrature-phase (Q) components, centred around
10 an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the signal to be received.

Background of the Invention

15 Most conventional radio receivers for use in portable communication devices such as cellular telephones, are of the super-heterodyne type in which a radio signal to be received is first down-converted to an intermediate frequency (which is still in the radio-frequency (rf) range) and then further down-converted to a base-band signal (having both I and Q components) from
20 which the information contained in the signal may be recovered. Such a receiver is robust. However, direct conversion receivers and, more recently, very low IF receivers have been proposed in order to reduce costs by eliminating both a relatively high performance, and therefore expensive, Surface Acoustic Wave (SAW) or crystal (in the case of AMPS, NADC or
25 other narrow-band systems) band-pass filter (for allowing the wanted IF signal to pass while blocking all unwanted IF signals in neighbouring channels) and one of the two rf local oscillators required in super-heterodyne receivers.

Direct conversion receivers immediately down convert the received radio
30 signal to a base-band signal thus completely eliminating the IF stage. However, such receivers suffer from the formation of a very large unwanted dc component interfering with the base-band signal. This dc component is formed largely by leakage from the local oscillator being received at the

receiver aerial together with the wanted signal, as well as offsets of amplifiers and mixers contained in the receivers.

In order to overcome this problem, a very low IF receiver has been proposed in which the received signal is first down-converted to be centred about an IF which is equal to half the channel spacing (i.e. half the bandwidth of the wanted signal), and then it is down-converted again to base-band. In this way, the dc component which is still formed when the first down-conversion takes place, is located (in frequency) at the very edge of the wanted signal.

From here, the unwanted dc component should be able to be relatively easily removed by suitable filtering of the dc component, without losing (very much) information contained in the wanted signal because of the dc component's location at the very edge of the wanted signal.

However, a problem with such an arrangement is that image signals from adjacent and even alternate channels can appear at base-band as unwanted noise interfering with the wanted signal. Such image signals result from imbalances in the analogue components of the I and Q paths between the first down-conversion and the analogue to digital conversion of the I and Q signals.

Summary of the Invention

According to a first aspect of the present invention, there is provided a complex multiplier for multiplying together a first input complex signal, having an In-phase, I, component and a Quadrature-phase, Q, component, and a second input complex signal and generating an output complex signal which is the product of the first and second input signals, the complex multiplier including a gain adjustment multiplier for adjusting the gain of one of the first signal's I and Q components relative to the other and a phase adjustment adder for adjusting the phase of one of the first signal's I and Q components relative to the other.

Preferably, the complex multiplier is a digital complex multiplier and the first and second input signals and the output signal are all digital signals having an associated sampling frequency, f_s .

5 Preferably, the complex multiplier (which from hereon may be referred to either as a complex multiplier, or as a complex balanced multiplier because of its ability to balance the I and Q components of the first input signal so as to have matching gains and phases) incorporates a quadrature phase generator for receiving a VLIF signal indicative of a Very Low Intermediate Frequency,
10 VLIF, by which the first input complex signal, after relative gain and phase adjustment, is to be down-converted, the quadrature phase generator being adapted to generate the second input complex signal from the VLIF signal. Furthermore, the quadrature phase generator also preferably includes the phase adjustment adder, wherein the phase adjustment adder acts to adjust
15 the phase of one or more of the components of the second input signal.

The VLIF signal may be a real (as opposed to complex) signal communicated to the quadrature phase generator from an external component (such as a controlling digital signal processor, or a VLIF local oscillator), or alternatively,
20 the VLIF signal may be internally generated by the quadrature phase generator itself (e.g. from an internal memory or an internal oscillator, etc.).

In one embodiment, the complex balanced multiplier has a second or higher order gain adjustment multiplier and a second or higher order phase
25 adjustment adder. Preferably, the complex balanced multiplier incorporates an adder arrangement which may be switched between an adding mode and an accumulating mode and which may operate at clocking speeds greater than the sampling frequency of the first input signal, whereby second and higher order terms of each complex multiplication may be calculated and
30 accumulated to first order terms during a single sampling period of the first input signal without requiring additional multipliers.

According to a second aspect of the present invention, there is provided a radio receiver comprising an rf mixer stage for receiving a wanted rf signal and down-converting it to a wanted complex VLIF signal centred around an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the wanted signal, an analogue to digital converter for converting the complex VLIF signal into a digital complex VLIF signal, and a complex multiplier as set out above for down-converting the digital complex VLIF signal to base-band.

Preferably, the VLIF about which the wanted signal is centred is between 10 and 20 per cent larger than half the channel spacing. Such a choice of IF is particularly advantageous for complex modulation schemes in which each symbol represents two or more bits, as will be required for the evolving standard known as EDGE (Enhanced Data-rate GSM Evolution), and corresponding standards in the US, as with these modulation schemes, it has been surprisingly discovered by the present inventors that significant information is contained in the edge portions of the signal (i.e. up to plus and minus half the channel spacing from the centre of the signal), the loss of which can give rise to an unacceptably large bit or block error rate. An example of a complex modulation scheme in which significant information is contained at the very edge of the channel is 8QPSK (8-position Quadrature Phase Shift Keying) where each symbol represents 3 bits. The term channel spacing, as will be well understood by a person skilled in the art, refers to the separation in terms of frequency between corresponding points in adjacent channels. For example, in GSM the channel separation is 200KHz.

Preferably, the VLIF signal is generated by a local oscillator which may advantageously be a fractional-N phase locked loop (fracNpll). Preferably, the fracNpll is a multi-accumulator fracNpll.

The complex multiplier according to the present invention is advantageous because it permits a difficulty associated with using a VLIF which is larger than half the channel spacing to be overcome. The difficulty is that as you increase the VLIF, you have to increase the band-width of the analogue to

digital converter (adc) and this in turn increases the amount of the negative alternate channel which is admitted by the adc and also increases the amount of this channel which, as an image, appears in the bandwidth of the wanted signal and which must be removed. By providing first or even second-order phase and gain adjustment means, it is possible to set the image rejection to zero (i.e. such that the amount of image components appearing in the base-band signal as noise after passing through the complex multiplier is substantially zero) for one (in the case of first order adjustment means) or even two or more (in the case of second or higher order adjustment means) specific frequencies. In this way, judicious setting of the adjustment means can minimise the effects of the negative alternate channel (which in many systems may in fact be much larger than either adjacent channel).

Setting of the adjustment means to provide for complete image rejection at a certain frequency or frequencies, hereafter referred to as calibration, can be done as a factory adjustment, or, where there is sufficient processing power available to the radio receiver, it could be done automatically by the radio receiver during detection of a known signal (e.g. a mid-amble), or a combination of both techniques could be used whereby an initial factory calibration is performed and then a processor associated with the radio receiver periodically checks the calibration and adjusts it if necessary. Preferably, the calibration is performed separately for a number of different ranges of operation of the radio receiver. For example, setting of the gain adjustment multiplier may be performed for a number of different levels of Automatic Gain Control (AGC) and setting of the phase adjustment adder may be performed for a number of different channels or ranges of channels.

Preferably, the adc takes the form of an over-sampled sigma-delta adc.

Preferably, the radio receiver is formed on an integrated circuit which advantageously includes transmission circuitry for transmitting signals. Ideally, the radio receiver and the transmission circuitry share a number of components such as the local oscillator.

Brief Description of the Drawings

In order that the present invention may be better understood, an embodiment thereof will now be described by way of example only, with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of a radio receiver in accordance with the present invention;

Figure 2 is a diagram illustrating the signal processing performed by the radio receiver of Figure 1 using a wanted GMSK signal and a single negative adjacent channel GMSK signal as an example input to the receiver;

Figure 3 is a diagram illustrating the signal processing performed by the radio receiver of Figure 1 using a wanted GMSK signal and a single negative alternate channel GMSK signal as an example input to the receiver;

Figure 4 is a block diagram of a first order complex balanced multiplier suitable for use in the receiver of Figure 1; and

Figure 5 is a block diagram similar to Figure 4 showing an alternative complex balanced multiplier suitable for use in the receiver of Figure 1.

Detailed Description of the Drawings

Referring to Figure 1, there is shown a Digital Very Low Intermediate Frequency (DVLIF) receiver 1 comprising a Radio Frequency (RF) portion 10, a Very Low Intermediate Frequency (VLIF) portion 30, and a base-band portion 60, with an RF mixer stage 20 located between the RF portion 10 and the VLIF portion 30, and a digital VLIF mixer stage 50 located between the VLIF portion 30 and the base-band portion 60. RF portion 10 comprises an aerial 12, an RF band-pass receive filter 14 and an amplifier 16. RF mixer

stage 20 comprises an In-phase (I) RF mixer 22, a Quadrature-phase (Q) RF mixer 24, a 90° RF phase shifter 26 and an RF Local Oscillator (LO) 28. VLIF portion 30 comprises I and Q IF amplifiers 31,32, I and Q low-pass anti-aliasing filters 33,34 I and Q sigma-delta modulators 35,36, and I and Q digital low pass filters 37,38. Digital VLIF mixer stage 50 comprises a complex balanced multiplier 51 operating as a digital IF mixer, and an IF LO 52. Base-band portion 60 is shown only comprising low pass I and Q digital selectivity filters 61 and 62, though it will of course further comprise the digital processing elements for decoding the digital signals, etc. as will be understood by a person skilled in the art.

The basic operation of the receiver of Figure 1 will now be described. The aerial 12 essentially captures all radio signals which impinge on it and these are fed to the receive filter 14 which attempts to filter away all signals which are outside the frequency range of interest. For example, if the receiver is intended for use as a GSM receiver, the receive filter 14 will greatly reduce the magnitude of all radio signals received by the aerial which are not within the GSM frequency range of 900MHz plus or minus 10% or so. The output from receive filter 14 is then amplified by amplifier 16 before being input to the RF mixing stage 20.

At the RF mixing stage 20, the signals output from the amplifier 16 are down-converted to a VLIF. RF LO 28 generates an RF signal whose frequency is such that the difference between it and the central frequency of the channel which the receiver is trying to receive is equal to the predetermined desired VLIF. The purpose of the 90° phase shifter 26 is to enable I and Q components of the down-converted signals to be output from the I and Q RF mixers 22,24. By generating I and Q components of the signal output by the amplifier 16, it becomes possible to consider the signal as a complex signal having real and imaginary components (corresponding to its I and Q components) and in this way it is possible to distinguish between signals having negative and positive frequencies respectively.

The I and Q signals output by the I and Q RF mixers 22,24 respectively are input to I and Q amplifiers 31,32 and I and Q low pass anti-aliasing filters 33,34 respectively. The purpose of these components is to remove all frequency components of signals arriving at the aerial 12 which are too high (when down-converted) to belong to the signal of interest (which when down-converted will lie approximately between dc and the channel spacing). In practice, because the filters 33,34 are simple (i.e. non-complex), they will also pass the signal contained in the negative adjacent channel (this is the channel located adjacent to the wanted channel substantially on the other side of the frequency of the RF signal generated by the RF LO 28). Furthermore, because real (i.e. non-ideal) filters do not have infinitely sharp cut-off points, the filters 33,34 (to avoid distorting the wanted signal) will also allow a substantial part of both the positive adjacent channel (the channel located adjacent to the wanted channel on the same side of the frequency of the RF signal generated by the RF LO 28 as the wanted channel) and the negative alternate channel (the channel located next but one to the wanted channel on the other side of the frequency generated by the RF LO 28, i.e. the channel adjacent to the negative adjacent channel referred to above).

The signals output from the filters 33,34 are then input to the I and Q sigma-delta modulators 35,36. The sigma-delta modulators 35,36, as will be well understood by a person skilled in the art, generate digital signals which correspond to the input analogue signals plus a large amount of high frequency noise. The digital signals output by the sigma-delta modulators 35,36 are therefore passed through digital low pass filters 37,38 whose purpose is to remove most of the high frequency noise generated by the sigma-delta modulators 35,36 so as to be left with a digital representation of the analog signals passed by the anti-aliasing low-pass filters 33,34 (i.e. the wanted channel, the negative adjacent channel and parts of the positive adjacent channel and the negative alternate channel).

These signals are then input to the digital VLIF mixer stage 50. The primary function of this stage is to further down-convert the wanted signal to base-band (i.e. centred about d.c. frequency). However, in the present invention, it

also performs the function of IQ balancing. IQ balancing means compensating the signals for variations in amplitude and phase between the I and Q components of the signals travelling through the analogue sections of the RF mixing stage 20 and the VLIF portion 30 which are introduced because of differences in the analogue components (or, more precisely, in the responses of the analogue components to the signals passing through them) in the I (22,31,33,35) and Q (24,32,34,36) paths respectively. If these imbalances are not compensated, it results in unwanted image components of signals other than the wanted signal appearing as noise in the same base-band channel as the wanted signal. The way in which this occurs is discussed in greater detail below. Note that the digital VLIF mixer stage 50 is shown as comprising a complex balanced multiplier 51 and an IF LO 52. The complete VLIF mixer stage 50 includes elements for providing the IQ balancing and these are considered as forming part of the complex balanced multiplier as opposed to the IF LO for the purposes of this invention though the exact choice of which component to associate them with is a little arbitrary as will be seen below. Furthermore, although the embodiments described in detail below show a hardware type implementation of complex balanced multipliers, it will be apparent to a person skilled in the art that a sufficiently powerful (in terms of Millions of Instructions Per Second (MIPS)) suitably programmed digital signal processor or microcontroller having a non-specific arithmetic and logic unit and memory. This will be discussed in greater detail below with reference to Figures 4 and 5.

The signals output from the digital VLIF mixer stage 50 are input to the I and Q digital low-pass selectivity filters 61,62 whose purpose is to remove all noise components outside the channel containing the wanted signal. The output from these filters will then typically be fed to a digital signal processor adapted to perform digital signal processing on the I and Q signals output by filters 61,62, such as equalisation, voice decoding etc.

Referring to Figure 2, an example of the signal response of the receiver of Figure 1 will now be described. The first frequency spectrum diagram of Figure 2 shows a wanted signal 100 and a negative adjacent signal 99

centred at 900.2 MHz and 900.0 MHz respectively, together with a dotted line representing the single tone signal 110 generated by RF LO 28. These signals represent typical GSM signals, thus each signal 99,100 has a GMSK spectrum and the channel spacing is 200KHz. According to a preferred

embodiment of one aspect of the present invention, the frequency of the RF LO signal 110 is chosen such that the wanted signal when down-converted will be centred about a VLIF which is slightly greater than half the channel spacing, and preferably between 1.1-1.2 times half the channel spacing.

Thus in Figure 2, the RF LO signal 110 is shown as being at a frequency of

900.085 MHz. This choice of frequency for the RF LO signal 110 results in the wanted signal 100 being centred about a VLIF of 115 KHz when down-converted by the RF mixer stage 50. A particularly preferred choice of the RF LO according to the present invention would be such as to give rise to the wanted signal being centred about a VLIF of 115.051 KHz which corresponds to $13 \text{ MHz}/24 * 435/2048$ as this frequency can be generated by a Multiple ACCumulator FRActional-N Phase Locked Loop (MACC FRAC-N PLL) frequency synthesiser. Such a frequency synthesiser is known in the art and is described in, for example, US patent No. 5,111,162 ["Digital Frequency Synthesizer having AFC and Modulation Applied to Frequency Divider,"

Hietala et al.].

The second frequency spectrum diagram (Figure 2B) of Figure 2 shows the signals 100,99 after having been down converted to a VLIF such that the wanted signal 100 is centred about a VLIF of 115 KHz. The negative adjacent signal is also down converted to a VLIF centred about -85 KHz (note that we are considering the signals as complex signals here which is why it is possible to distinguish between a negative and a positive frequency). Also shown in Figure 2B is a substantially d.c. signal 120 which is referred to as the IM2 (second order intermodulation) signal. The IM2 signal is noise which is generated by a combination of leakage from the RF LO being detected by the aerial 12 and re-combining in essence with itself at the RF mixer stage 20, and second order non-linearities in the analogue mixers 22,24. The effect of filters 33,34 is also shown in Figure 2B by the filter response curve 130.

Because filters 33,34 are real filters, their frequency response is symmetrical about d.c. In order to avoid clipping or distorting the wanted signal 100, the corner frequency of the filters is set beyond 215 KHz. This results in substantially all of the negative adjacent channel 99 (which does not extend much beyond -185 KHz) being passed by these filters 33,34.

Figure 2B also shows some image signals 99',100' which can be referred to as the negative adjacent signal image 99' and the wanted signal image 100'. The negative adjacent signal image 99' is centred around +85KHz while the wanted signal image 100' is centred around -115KHz. These image signals result from imbalances between the I and Q paths, which result, in turn, from imbalances in the analogue components (most precisely in the frequency responses of such components) contained in the different I and Q paths.

The final frequency spectrum diagram (Figure 2C) of Figure 2 shows the wanted 100, negative adjacent 99 and IM2 120, and image 99',100' signals having been further down-converted by the digital VLIF mixer stage 50 such that the wanted signal 100 is now at base-band (i.e. centred about d.c.) and is in a digital format. The negative adjacent signal has been further down-converted and is centred at -200 KHz, while the IM2 signal is located at -115 KHz. The fact that the IM2 signal is located 115 KHz away from the centre of the wanted signal is a critical advantage of the receiver according to the present invention as it permits this signal to be filtered out by either a low pass filter or a notch filter without clipping or distorting the wanted signal 100.

Figure 2C also shows the image signals 99',100' which have also be down-converted by -115 KHz such that the negative adjacent signal image 99' is now centred about -30 KHz and the wanted signal image 100' is now centred about -230 KHz. The image signals are also shown as having been reduced in magnitude from Figure 2B, as a result of the I,Q balancing of the VLIF mixer stage 50. This I,Q balancing is the second function of the VLIF mixer stage 50. In practice, the I,Q balancing of the VLIF mixer stage 50 can only be performed substantially perfectly at a particular frequency (or at a few distinct frequencies), however, for the sake of clarity and in order to better see where the optimum frequency or frequencies would be, this notchiness effect

of the VLIF mixer stage is not shown in Figures 2c and 3C. Clearly, the wanted signal image 100' is well separated from the wanted signal 100 (which does not extend substantially beyond ± 100 KHz), and thus it would not be worthwhile maximising the balancing of the VLIF mixer stage at this frequency, however the negative adjacent channel image 99' is centred about -30 KHz and will appear in the wanted signal as noise, and thus it might be worthwhile maximising the balancing of the VLIF mixer stage at the central frequency of the negative adjacent signal image 99'.

Referring now to Figure 3, a second example of the signal response of the receiver of Figure 1 will now be described, in which wanted signal 100 and a negative alternate signal 98 centred at 900.2 MHz and 899.8 MHz respectively, are shown arriving at aerial 12 (together with a dotted line representing the single tone signal 110 generated by RF LO 28) in place of the wanted 100 and negative adjacent 99 signals. Of course, when operating in a real environment, the wanted signal 100 will be received together with a large number of other signals including both a negative adjacent and a negative alternate signal; however, for the sake of clarity, Figures 2 and 3 consider only one signal, in addition to the wanted signal, at a time.

The negative alternate signal 98 is spaced from the wanted signal 100 by 400 KHz. The negative alternate signal 98 is shown as being much larger than the wanted signal 100 because, according to the GSM Specifications, an alternate channel can contain signals whose total power is up to 41dB greater than that of the wanted signal 100 as a result of re-use provisions of the cellular structure of a GSM network.

From the second frequency spectrum diagram (Figure 3B) of Figure 3, it can be seen that although a large part of the down-converted negative alternate signal 98 will be filtered by the filters 33,34 (whose frequency response is again shown in Figure 3 by the filter response curve 130), the signal power of the remainder of the negative alternate signal 98 which is still passed by the filters 33,34 is none-the-less significantly large. The main reason for this is simply that the negative alternate signal is just so much bigger than the

wanted signal that even after its power is reduced by the action of the filters it will still be significantly large. Furthermore, since these signals are all Gaussian in terms of their signal strength frequency distribution, and since the negative alternate signal is just so large, its components outside its allotted channel (i.e. spreading into the negative adjacent channel) will also represent a significant level of noise which must be taken into account when designing a receiver.

From the third frequency spectrum diagram (Figure 3C) of Figure 3, it can be seen that for a reasonable amount of imbalance between the I and Q paths of the receiver, and without any balancing being performed by the complex balanced multiplier 51, a relatively large portion of the negative alternate signal image 98' appears in the wanted channel after conversion to base-band (note that image signals 98',100' should really have been included in Figure 3B but have been omitted for the sake of clarity). By comparing Figure 3C with Figure 2C, it is apparent that the negative alternate image 98' will potentially present a greater amount of unwanted noise within the wanted channel than the negative adjacent signal image 99' will. Furthermore, it is apparent that the two images peak at different frequencies (Again, the effect of the balancing of the VLIF mixer stage being effective at only one or a few distinct frequencies is not shown in Figure 3C). Thus, the complex balanced multiplier should preferably be able to perform IQ balancing in such a way as to minimise the effect of at least the negative alternate signal image and ideally both the negative alternate and the negative adjacent signal images.

Figure 4 shows a first order complex balanced multiplier 500. The complex balanced multiplier 500 comprises a quadrature phase generator 510; a Q-path gain adjustment means 520; first, second, third and fourth multipliers 531,532,533,534; and first and second adder/subtractors 541,542.

Quadrature phase generator 510 receives a VLIF signal in the form of a phase signal O_{sd} from the IF LO 52 and a programmable Q-path phase correction β as inputs, and outputs $\cos(O_{sd})$, $\sin(O_{sd})$, $\cos(O_{sd} + \beta)$ and $\sin(O_{sd} + \beta)$ signals, which are applied to the second inputs of the first, second, third and fourth multipliers 531,532,533,534 respectively; additionally, the first and second multipliers 531,532 have the digital I-path signal lin

(output from the digital I filter 37 of Figure 1) applied to their first inputs; while the third and fourth multipliers 533,534 have the digital Q-path signal Q_{in} (output from the digital Q filter 38 of Figure 1) applied to their first inputs. The outputs of the first and fourth multipliers 531,534 are applied as inputs to the first adder/subtractor 541 which outputs a digital baseband I signal I_{out} ; while the outputs of the second and third multipliers 532,533 are applied as inputs to the second adder/subtractor 542 which outputs a digital baseband Q signal Q_{out} .

- 10 The effect of the complex balanced multiplier 500 is to generate output I and Q signals I_{out} and Q_{out} from input signals I_{in} , Q_{in} and O_{sd} , as set out in equation 1 below:-

$$I_{out} + jQ_{out} = (I_{in} + jA_d \cdot e^{j\beta} \cdot Q_{in}) \cdot e^{+jO_{sd}} \quad \text{Equation 1}$$

15

From Equation 1, it can be seen that if Q_{in} differs from what it is supposed to be because of relative imbalances between the I and Q paths by $1/A_d$ in gain and $-\beta$ in phase, then the effect of the complex balanced multiplier 500 is to correct the imbalance as desired. Unfortunately, the imbalance between the paths will not be constant over frequency. Thus the complex balanced multiplier 500 of Figure 1 is only able to exactly balance the I and Q paths at a single frequency. In order to fully describe the imbalance between the paths created by the differences in the analogue components contained in these paths, one must consider the imbalances as being caused by a filter having a

20

25 Finite Impulse Response (FIR) given by Equation 2 below:-

$$H_{imbalance}(z) = \frac{1}{A_{d0}} \cdot e^{-j\beta_0} + \frac{1}{A_{d1}} \cdot e^{-j\beta_1} \cdot z^{-1} + \frac{1}{A_{d2}} \cdot e^{-j\beta_2} \cdot z^{-2} + \dots \quad \text{Equation 2}$$

- Clearly, to counter the effect of such an FIR one needs to provide a filter or equivalent means having the response given by Equation 3 below:-
- 30

$$H_{balance}(z) = A_{d0} \cdot e^{+j\beta_0} + A_{d1} \cdot e^{+j\beta_1} \cdot z^{-1} + A_{d2} \cdot e^{+j\beta_2} \cdot z^{-2} + \dots \quad \text{Equation 3}$$

From equation 3, it is apparent that the first-order compensation provided by complex balanced multiplier 500 corresponds to the first term of H_{balance} . In order to provide higher-order compensation or balancing, one could provide a dedicated digital filter having an FIR to compensate for the imbalance up to as many orders as desired. However, it is preferable to re-use some of the elements of the complex multiplier contained within the digital VLIF mixer stage 50.

Figure 5 illustrates a complex balanced multiplier 600 in which some parts are re-used to enable a higher-than-first-order FIR to be performed which can compensate for the imbalance between the I and Q paths at more than one frequency (note that generally speaking, a second order FIR will be able to compensate the imbalance at 2 specific frequencies exactly, while a third order FIR can compensate at 3 specific frequencies, etc.). Specifically, Figure 5 illustrates a fourth order complex balanced multiplier, however, it will be readily apparent to the reader that the arrangement may be modified to alter the order of the FIR of the arrangement, the major constraint being the clock speed available to the re-used elements compared to the sample frequency of the input I and Q signals.

Complex balanced multiplier 600 comprises a Q_{in} storage register 601 and an associated multiplex means 602; a quadrature phase generator 610 and a phase correction β_i storage register 611; a Q-path gain adjustment means 620 and a gain adjustment A_{D_i} storage register 621; first, second, third and fourth multipliers 631,632,633,634; first and second adder/subtractors 641,642; I_{out} and Q_{out} storage registers 651,652; and first and second switches 661,662.

The operation of complex balanced multiplier 600 is as follows. The I and Q signals input to the complex balanced multiplier 600 are in the form of digital sampled values. If one considers the sampled values $I_{\text{in}0}$, $Q_{\text{in}0}$, $Q_{\text{in}-1}$, $Q_{\text{in}-2}$, $Q_{\text{in}-3}$ where $I_{\text{in}0}$ and $Q_{\text{in}0}$ are the values of I_{in} and Q_{in} at time $t=0$, $Q_{\text{in}-1}$ is the preceding sampled value of Q_{in} at time $t=-T_s$, $Q_{\text{in}-2}$ is the value of Q_{in} at time

$t = -2\tau_s$, etc., where τ_s is the inverse of the sampling frequency f_s . Q_{in} storage 601 stores the 3 preceding sample values of Q_{in} , namely Q_{in-1} , Q_{in-2} , Q_{in-3} . The associated multiplex means 602 has 4 inputs (namely Q_{in0} , Q_{in-1} , Q_{in-2} , Q_{in-3}) any one of which it can choose to form the output which is passed on to the gain adjustment means 620. Gain adjustment means 620 multiplies together the 2 values appearing at its two inputs, namely the output from multiplex means 602 and the output from the gain adjustment A_{Di} storage register 621 which stores gain adjustment coefficients A_{D0} , A_{D1} , A_{D2} , A_{D3} .

Quadrature phase generator 610 receives as inputs signals O_{sd} and the output from the phase correction β_i storage register 611. The signals output by the quadrature phase generator 610 are $\cos(O_{sd})$ and $\sin(O_{sd})$ which are output at a rate of f_s and $\cos(O_{sd} + \beta_i)$ and $\sin(O_{sd} + \beta_i)$ which are output at a rate of $4f_s$. The signals $\cos(O_{sd})$, $\sin(O_{sd})$, $\cos(O_{sd} + \beta)$ and $\sin(O_{sd} + \beta)$ are applied to the second inputs of the first, second, third and fourth multipliers 631, 632, 633, 634 respectively; additionally, the first and second multipliers 631, 632 have the digital I-path signal I_{in0} (output from the digital I filter 37 of Figure 1) applied to their first inputs; while the third and fourth multipliers 633, 634 have the output of the gain adjustment means 620 applied to their first inputs. The output of the first multiplier 631 is applied to a first terminal of the first switch 661; the output of the second multiplier 632 is applied to a first terminal of the second switch 662; the output of the third multiplier 633 is applied as an input to the second adder/subtractor 642; and the output of the fourth multiplier 634 is applied as an input to the first adder/subtractor 641. The output of the first adder/subtractor 641 is applied to the I_{out} storage register 651 and the output of the second adder/subtractor 642 is applied to the Q_{out} storage register 652. The output of the I_{out} storage register 651 forms the I_{out} output of the complex balanced multiplier 600 and is additionally fed-back to a second terminal of the first switch 661. The output of the Q_{out} storage register 652 forms the Q_{out} output of the complex balanced multiplier 600 and is additionally fed-back to a second terminal of the second switch 662. First switch 661 acts to connect either its first terminal or its second terminal to an input to the first adder/subtractor 641. Second switch

662 acts to connect either its first terminal or its second terminal to an input of the second adder/subtractor. It will be apparent to the reader that when either switch 661,662 is connecting the input to the respective adder/subtractor to the second terminal of the switch, that the adder/subtractor together with the
 5 respective storage register will act as an accumulator with the running total being stored in the respective storage register.

Consider now that the desired outputs from the complex balanced multiplier 600 are given by equation 4 below:-

$$I_{out} + jQ_{out} = (I_{in0} + jQ_{in0} \cdot A_{D0} \cdot e^{j\beta_0} + jQ_{in-1} \cdot A_{D1} \cdot e^{j\beta_1} + \dots + jQ_{in-3} \cdot A_{D3} \cdot e^{j\beta_3}) e^{jO_{sd}}$$

(Equation 4)

In order to achieve the I_{out} and Q_{out} signals given by this equation, the
 15 complex balanced multiplier operates four cycles in every sampling period T_s . In the first cycle, the terms $I_{in0} \cdot e^{jO_{sd}}$ and $jQ_{in0} \cdot A_{D0} \cdot e^{j\beta_0} \cdot e^{jO_{sd}}$ are calculated. To do this, multiplex means 602 selects its first input which receives Q_{in0} as its output and gain adjustment storage register 621 outputs gain adjustment constant A_{D0} which is then multiplied with Q_{in0} at the gain adjustment means
 20 620 to generate $Q_{in0} \cdot A_{D0}$. Also phase adjustment storage register 611 outputs β_0 which is used by the quadrature phase generator 610 to generate the real (cos) and imaginary (sin) components of $e^{jO_{sd}}$ and $e^{j(\beta_0 + O_{sd})}$ respectively. These components are appropriately multiplied with I_{in0} and Q_{in0} in multipliers 631 to 634 and the real and imaginary terms are appropriately added together
 25 in adder/subtractors 641 and 642 to produce the real and imaginary parts of $(I_{in0} + jQ_{in0} \cdot A_{D0} \cdot e^{j\beta_0}) \cdot e^{jO_{sd}}$ respectively. These are then stored in the I_{out} and Q_{out} storage registers 651,652 respectively and the first cycle comes to an end.

30 During the second cycle, first and second switches 661,662 are switched into their second state such that the output of the storage registers 651,652 are fed back to the first inputs of the adder/subtractors 641,642. Also, multiplex means 602 selects its second input which receives Q_{in-1} from Q_{in} storage

register 601 as its output; gain adjustment storage register 621 outputs A_{D1} to gain adjustment means 620; and phase adjustment means 611 outputs β_1 to the quadrature phase generator 610 which generates real and imaginary components of $e^{j(\beta_1 + O_{sd})}$ which are multiplied with the output of gain adjustment means 620 (i.e. $Q_{in-1} * A_{D1}$) in multipliers 633 and 634 to generate imaginary and real components of the term $jQ_{in-1} * A_{D1} * e^{j(\beta_1 + O_{sd})}$ which are accumulated to the values stored in storage registers 652 and 651 respectively; the new totals are then restored in registers 652 and 651 ready for the third and fourth cycles.

The third and fourth cycles proceed in an analogous way to the second cycle until all of the components required by Equation 4 have been calculated whereupon signals I_{out} and Q_{out} become valid; switches 661 and 662 are returned to their first positions; and new sample values of I_{in} , Q_{in} and O_{sd} are received at the inputs to the complex balanced multiplier 600.

It will by now be apparent to the reader that the present invention provides a complex balanced multiplier which permits a radio receiver architecture which has all of the advantages of a direct conversion receiver in terms of the lack of an expensive SAW filter and a second rf local oscillator, and which is nonetheless able to receive narrow-band (e.g. 200KHz) radio-signals having greater than first order modulation (i.e. 2 or more bits per symbol) transmitting symbols at rates of the order of 20-30 thousand symbols per second (in which the adjacent and alternate channels may contain noise having a significantly greater magnitude than the magnitude of the wanted signal, in accordance with GSM specifications or similar). The complex balanced multiplier permits the use of a local oscillator which down-converts the wanted signal to a VLIF centred about a frequency which is between 1.1 and 1.2 times half the channel spacing. The use of a complex balanced multiplier according to the present invention to perform the VLIF to base-band down-conversion minimises the additional amount of noise placed into the wanted signal channel at base-band from the negative alternate image channel as a result of this choice of VLIF. Optimally, a second or higher order balanced complex multiplier is used which permits substantially perfect image rejection at two or

more frequencies which may be pre-programmed to minimise the effects of noise from unwanted image signals.

The complex balanced multipliers of Figures 4 and 5 are examples of possible implementations only and alternative implementations will be readily apparent to persons skilled in the art. For example, instead of using a serial implementation to generate a greater than first order adjustment means, one could use a parallel implementation in which more real multipliers are used to generate the higher order terms in parallel with the first order terms.

Alternatively, one could simply employ a non-specific digital signal processor (dsp) or microcontroller suitably programmed to perform the desired complex multiplications with the relevant IQ balancing operations incorporated therein. Obviously, for applications such as GSM or EDGE a very powerful digital signal processor (in terms of its MIPS, relative to today's standards) would be required which would make it an unattractive solution at present but obviously if dsp's continue to become cheaper and more powerful it may be a viable solution in the future.

20
CLAIMS

1. A complex multiplier for multiplying together a first input complex signal, having an In-phase, I, component and a Quadrature-phase, Q, component, and a second input complex signal and generating an output complex signal which is the product of the first and second input signals, the complex multiplier including a gain adjustment multiplier for adjusting the gain of one of the first signal's I and Q components relative to the other and a phase adjustment adder for adjusting the phase of one of the first signal's I and Q components relative to the other.
2. A complex multiplier as claimed in claim 1 wherein the complex multiplier is a digital complex multiplier and the first and second input signals and the output signal are all digital signals having an associated sampling frequency, f_s .
3. A complex multiplier as claimed in either one of the preceding claims including a quadrature phase generator for receiving a VLIF signal indicative of a Very Low Intermediate Frequency, VLIF, by which the first input complex signal, after relative gain and phase adjustment, is to be down-converted, the quadrature phase generator being adapted to generate the second input complex signal from the VLIF signal.
4. A complex multiplier as claimed in claim 3 wherein the quadrature phase generator includes the phase adjustment adder, wherein the phase adjustment adder acts to adjust the phase of one or more of the components of the second input signal, to thereby adjust the phase of one of the I and Q components of the first input signal.
5. A complex multiplier as claimed in any one of the preceding claims wherein the gain adjustment multiplier is a second or higher order gain adjustment multiplier and the phase adjustment adder is a second or higher order phase adjustment adder.

6. A complex multiplier as claimed in any one of the preceding claims further comprising an adder arrangement which may be switched between an adding mode and an accumulating mode and which may operate at clocking speeds greater than the sampling frequency of the first input signal, whereby
5 second and higher order terms of each complex multiplication may be calculated and accumulated to first order terms during a single sampling period of the first input signal without requiring additional multipliers

7. A radio receiver comprising an rf mixer stage for receiving a wanted rf
10 signal and down-converting it to a wanted complex VLIF signal centred around an Intermediate Frequency (IF) which is of the same order of magnitude as the bandwidth of the wanted signal, an analogue to digital converter for converting the complex VLIF signal into a digital complex VLIF signal, and a complex multiplier as claimed in any one of the preceding claims
15 for down-converting the digital complex VLIF signal to base-band.

8. A radio receiver as claimed in claim 7 wherein the gain adjustment multiplier and the phase adjustment adder, of the complex multiplier as claimed in any one of claims 1-6, are adapted to provide close to perfect
20 balancing at a frequency close to an edge of the base-band frequency spectrum whereby the amount of the image signal from the negative alternate channel is minimised.

9. A radio receiver as claimed in either one of claims 7 or 8 wherein the IF
25 about which the wanted VLIF signal is centred is between 10 and 20 per cent larger than half the channel spacing.

10. A radio receiver as claimed in any one of claims 7, 8 or 9 wherein the local oscillator is a fractional-N phase locked loop frequency synthesiser.
30

11. A radio receiver as claimed in claim 10 wherein the fractional-N phase locked loop frequency synthesiser incorporates two or more accumulators.

12. A radio receiver as claimed in any one of claims 7 to 11 wherein the analogue to digital converter takes the form of an over-sampled sigma delta analogue to digital converter.
- 5 13. A radio receiver as claimed in any one of claims 7 to 12 formed as an integrated circuit.

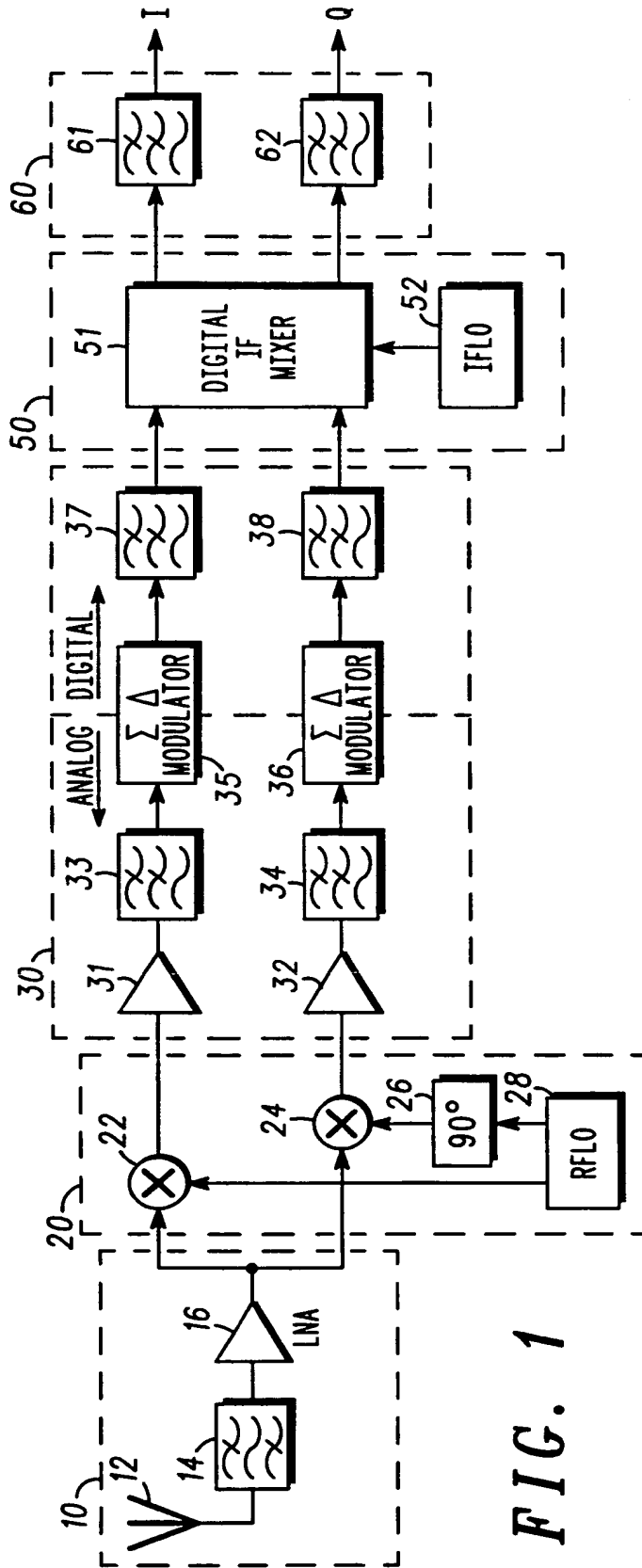


FIG. 1

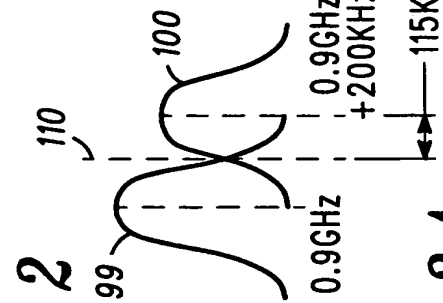


FIG. 2A

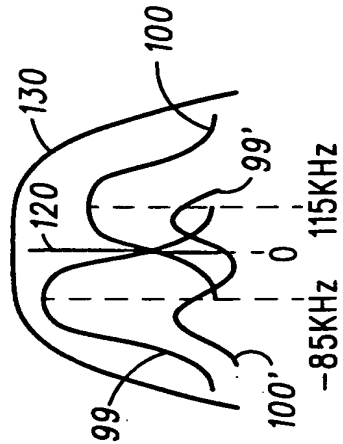


FIG. 2B

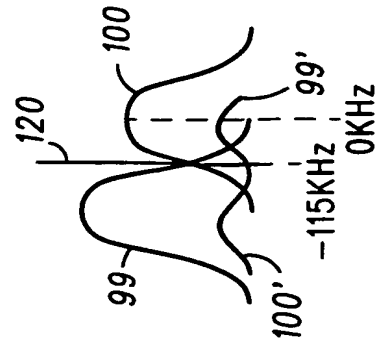


FIG. 2C

FIG. 3

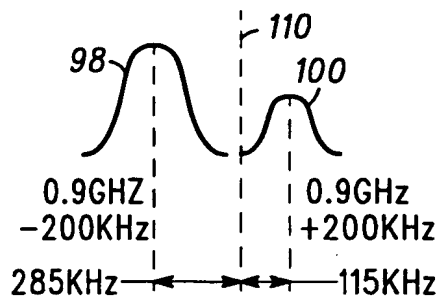


FIG. 3A

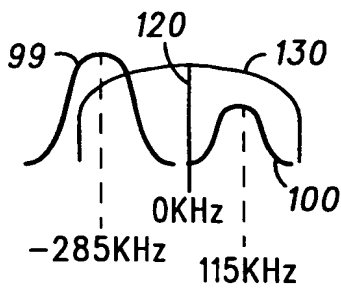


FIG. 3B

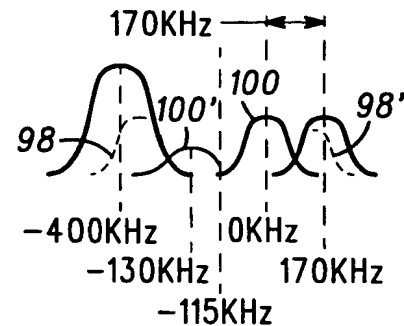


FIG. 3C

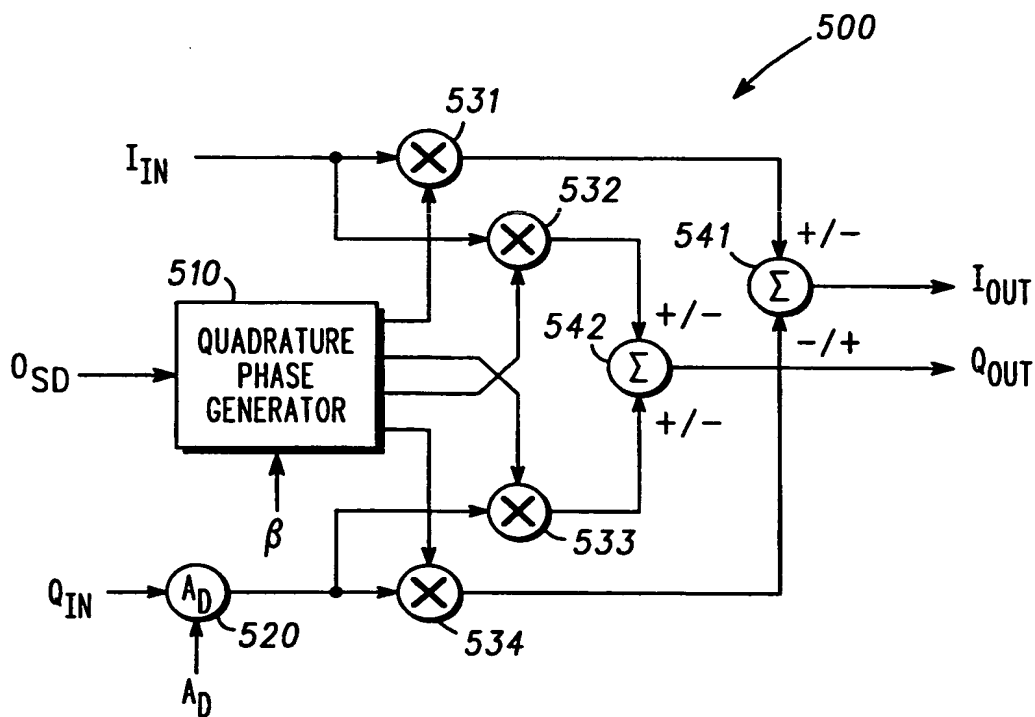


FIG. 4

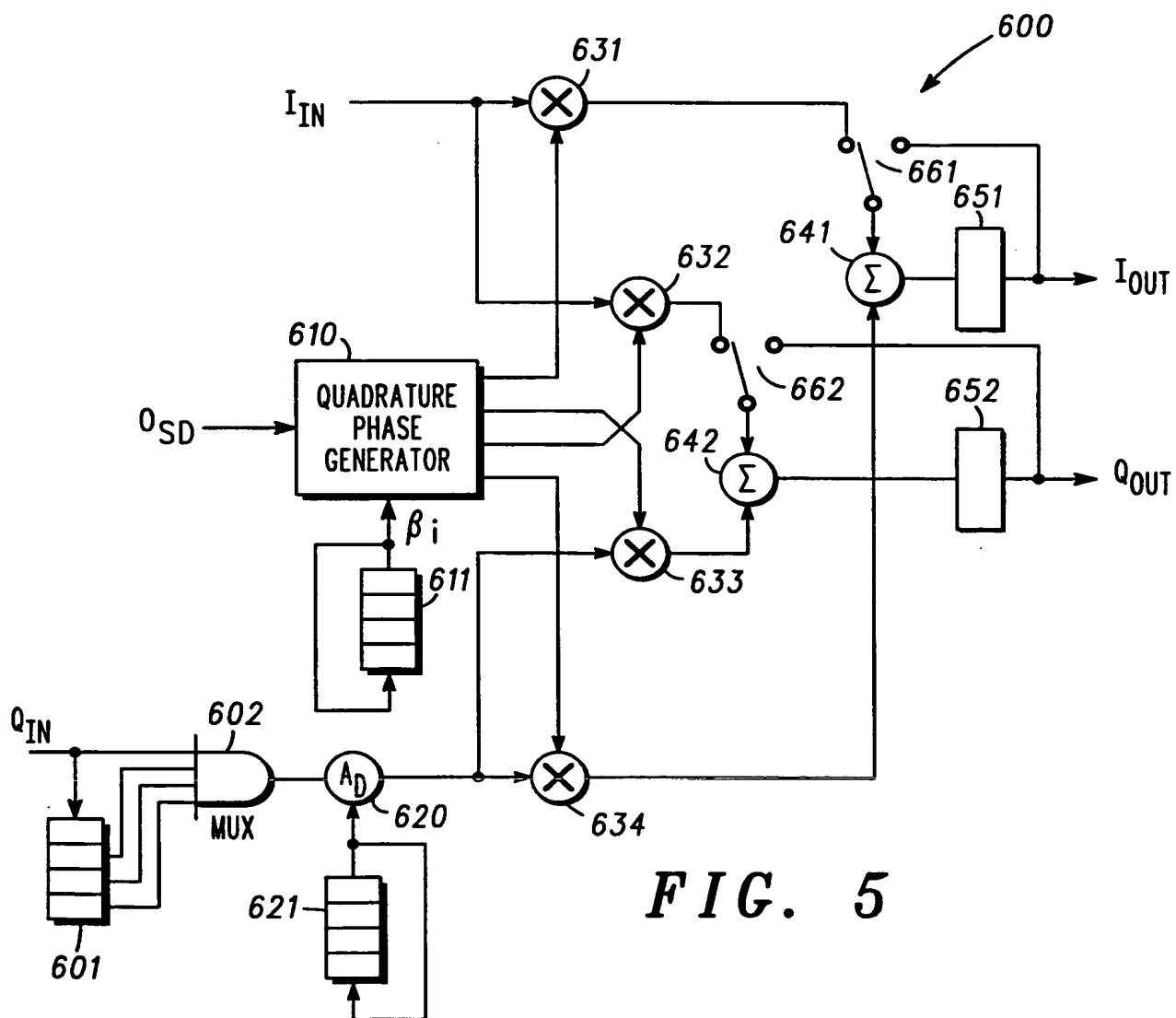


FIG. 5

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 00/05148

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H03D3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 878 089 A (DAPPER MARK J ET AL) 2 March 1999 (1999-03-02) column 4, line 11 -column 5, line 20; figure 2	1-3,7
A	US 4 688 096 A (CAMPBELL III EDWARD R ET AL) 18 August 1987 (1987-08-18) figures 1,3	1,7
A	WO 94 29948 A (RCA THOMSON LICENSING CORP ;ASCHWANDEN FELIX (CH)) 22 December 1994 (1994-12-22) abstract; figure 5	4
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

8 September 2000

Date of mailing of the international search report

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Peeters, M

INTERNATIONAL SEARCH REPORT

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